IN THE CLAIMS

Please cancel Claim 1, without prejudice.

Please amend Claim 3, as follows.

Please add new Claims 4 and 5, as follows.

Claim 1. (Cancelled)

Claim 2. (Original) A method for implementing a segmentation operation comprising the steps of:

providing a first segment selector for deriving a linear address of a segment descriptor in a first descriptor table,

providing a second segment selector for deriving a linear address of a segment descriptor in a second descriptor table,

attempting an access of the first descriptor table to derive a segment descriptor,

attempting an access of the second descriptor table to derive a segment descriptor if the access of the first descriptor table fails, and

storing a derived segment descriptor from a successful attempted access in a descriptor register.

Claim 3. (Currently Amended) A method as claimed in Claim 2 in which any attempt to access is divided into discrete sub-steps comprising:

checking properties of a logical address to determine whether those properties are consistent with the criteria for addressing [[a]] <u>one of the</u> first <u>and the second</u> descriptor table<u>s</u> in a first discrete sub-step of deriving a linear address, and

performing a base-add operation to determine the linear address as a second discrete sub-step of deriving a linear address.

Claim 4. (New) A microprocessor that implements a segmentation operation, comprising:

a first descriptor table operable to store segment descriptors;

a second descriptor table operable to store segment descriptors;

a first register operable to hold a first segment selector operable to derive a linear address of a segment descriptor in the first descriptor table;

a second register operable to hold a second segment selector operable to derive a linear address of a segment descriptor in the second descriptor table; and

a descriptor register operable to store a derived segment descriptor from a successful attempted access of one of said first descriptor table and said second descriptor table;

wherein said microprocessor is operable to:

attempt an access of the first descriptor table to derive a segment descriptor;

if the access of the first descriptor table fails, attempt an access of the second descriptor table to derive a segment descriptor; and

store in the descriptor register a derived segment descriptor from a successful attempted access.

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Claim 5. (New) The microprocessor as claimed in Claim 4, further comprising:

a first base register operable to store a first base address; and

a second base register operable to store a second base address;

wherein said microprocessor is further operable to divide attempts to access into discrete sub-steps by:

checking properties of a logical address to determine whether those properties are consistent with criteria for addressing one of the first and the second descriptor tables in a first discrete sub-step of deriving a linear address; and

performing a base-add operation to determine the linear address as a second discrete sub-step of deriving a linear address, said performing including accessing a value from one of the first and the second base registers.